

CLAIMS

Having thus described our invention in detail, what we claim is new and desire to secure by the letters Patent is:

- 1 1. A method of improving the SiGe bipolar yield of a SiGe heterojunction bipolar
2 transistor comprising the steps of:
3
4 (a) forming a passivation layer on at least exposed sidewalls of an emitter, said emitter
5 is in contact with an underlying SiGe base region through an emitter opening formed
6 in an insulator layer; and
7
8 (b) siliciding exposed silicon surfaces so as to form silicide regions therein.
- 1 2. The method of Claim 1 wherein said passivation layer is formed from a rapid
2 thermal chemical vapor deposition process.
- 1 3. The method of Claim 1 wherein said passivation layer is composed of a nitride, an
2 oxide, an oxynitride or any combination thereof.
- 1 4. The method of Claim 1 wherein said passivation layer is a nitride passivation layer.
- 1 5. The method of Claim 4 wherein said nitride passivation layer is formed from a
2 rapid thermal chemical vapor deposition process which is carried out in a nitrogen-
3 containing atmosphere.
- 1 6. The method of Claim 5 wherein said nitrogen-containing atmosphere is selected
2 from the group consisting of NO, N₂O and N₂.
- 1 7. The method of Claim 4 wherein said rapid thermal chemical vapor deposition
2 process is carried out at a temperature of about 700°C or greater.
- 1 8. The method of Claim 1 wherein said SiGe base region is formed by a deposition
2 process selected from the group consisting of ultra-high vacuum chemical vapor

3 deposition (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor
4 deposition (RTCVD) and plasma-enhanced chemical vapor deposition.

1 9. A SiGe heterojunction bipolar transistor comprising:
2

3 a semiconductor substrate having a collector and subcollector region formed therein,
4 wherein said collector is formed between isolation regions that are also present in the
5 substrate;
6

7 a SiGe layer formed on said substrate, said SiGe layer including polycrystalline Si
8 regions formed above said isolation regions and a SiGe base region formed above said
9 collector and subcollector regions;
10

11 a patterned insulator layer formed on said SiGe base region, said patterned insulator
12 layer having an opening therein;
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14 an emitter formed on said patterned insulator layer and in contact with said SiGe base
15 region through said opening, said emitter having exposed sidewalls;
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17 a conformal passivation layer formed on at least said exposed sidewalls of said
18 emitter; and
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20 silicide regions formed on exposed portions of said SiGe layer and said emitter not
21 covered by said conformal passivation layer.

1 10. The SiGe heterojunction bipolar transistor of Claim 9 wherein said semiconductor
2 substrate is selected from the group consisting of Si, Ge, SiGe, GaAs, InAs, InP, other
3 III/V compound semiconductors, Si/Si and Si/SiGe.

1 11. The SiGe heterojunction bipolar transistor of Claim 9 wherein said emitter is
2 composed of intrinsic polysilicon.

1 12. The SiGe heterojunction bipolar transistor of Claim 9 wherein said patterned
2 insulator is composed of SiO₂ or Si oxynitride.

1 13. The SiGe heterojunction bipolar transistor of Claim 9 wherein said patterned
2 insulator is composed of multi-insulator layers.

1 14. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation
2 layer is also formed on vertical sidewalls of said patterned insulator and portions of
3 said SiGe base region.

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4 15. The SiGe heterojunction bipolar transistor of Claim 9 wherein said silicide
5 regions are formed in an exposed horizontal surface of said emitter, said
6 polycrystalline Si region and a portion of said SiGe base region.

1 16. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation
2 layer is composed of a nitride, an oxide, an oxynitride or any combination thereof.

1 17. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation
2 layer is a nitride passivation layer.

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